(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 002 369 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
29.05.2002 Bulletin 2002/22

(21) Application number: **98906163.5**

(22) Date of filing: **11.02.1998**

(51) Int Cl.[7]: **H03L 7/081**, G11C 7/00

(86) International application number:
PCT/US98/02234

(87) International publication number:
WO 98/35446 (13.08.1998 Gazette 1998/32)

(54) SYNCHRONOUS CLOCK GENERATOR INCLUDING DELAY-LOCKED LOOP

SYNCHRONER TAKTGENERATOR MIT VERZÖGERUNGSREGELSCHLEIFE

HORLOGE SYNCHRONE AVEC BOUCLE A RETARD DE PHASE

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **11.02.1997 US 799661**

(43) Date of publication of application:
24.05.2000 Bulletin 2000/21

(73) Proprietor: **Micron Technology, Inc.**
Boise, ID 83706-0006 (US)

(72) Inventors:
- **HARRISON, Ronnie, M.**
  Boise, ID 83716 (US)
- **KEETH, Brent**
  Boise, ID 83704 (US)

(74) Representative: **Hirsch, Peter, Dipl.-Ing.**
Klunker Schmitt-Nilson Hirsch
Winzererstrasse 106
80797 München (DE)

(56) References cited:
EP-A- 0 476 585 **EP-A- 0 704 848**

- **YASUO ARAI ET AL: "A CMOS FOUR-CHANNEL X 1K TIME MEMORY LSI WITH 1-NS/B RESOLUTION" IEEE JOURNAL OF SOLID-STATE CIRCUITS., vol. 27, no. 3, 1 March 1992, NEW YORK US, pages 359-364, XP000295888**
- **ARAI Y ET AL: "TMC - A CMOS TIME TO DIGITAL CONVERTER VLSI" IEEE TRANSACTIONS ON NUCLEAR SCIENCE., vol. 36, no. 1, 1 February 1989, NEW YORK US, pages 528-531, XP000112427**
- **ARAI Y ET AL: "A TIME DIGITIZER CMOS GATE-ARRAY WITH A 150 PS TIME RESOLUTION" IEEE JOURNAL OF SOLID-STATE CIRCUITS., vol. 31, no. 2, 1 February 1996, NEW YORK US, pages 212-220, XP000597207**

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 1 002 369 B1

Description

TECHNICAL FIELD

[0001] The present invention relates to a memory device adapted to receive data and commands at a reference frequency, it relates also to a method of controlling the latching of commands and data.

BACKGROUND OF THE INVENTION

[0002] Many high-speed integrated circuit devices, such as synchronous dynamic random access memories (SDRAM), rely upon clock signals to control the flow of commands, data, and addresses into, through, and out of the devices. Typically, operations are initiated at edges of the clock signals (*i.e.*, transitions from high to low or low to high). To more precisely control the timing of operations within the device, each period of a clock signal is sometimes divided into subperiods so that certain operations do not begin until shortly after the clock edge.

[0003] One method for controlling the timing of operations within a period of a clock signal generates phase-delayed versions of the clock signal. For example, to divide the clock period into four subperiods, phase delayed versions are produced that lag the clock signal by 90°, 180° and 270°, respectively. Edges of the phase-delayed clock signals provide signal transitions at the beginning or end of each subperiod that can be used to initiate operations.

[0004] An example of such an approach is shown in Figures 1 and 2 where the timing of operations in a memory device 10 is defined by an externally provided reference control clock signal CCLKREF and an externally provided reference data clock signal DCLKREF. The reference clock signals CCLKREF, DCLKREF are generated in memory controller 11 and transmitted to the memory device 10 over a command clock bus and a data clock bus. The reference clock signals CCLKREF, DCLKREF have identical frequencies, although the reference control clock signal CCLKREF is a continuous signal and the reference data clock signal DCLKREF is a discontinuous signal, *i.e.,* the reference data clock signal DCLKREF does not include a pulse for every clock period T, as shown in Figure 2. Although the reference clock signals CCLKREF, DCLKREF have equal frequencies, they may be phase shifted by a lag time T_L upon arrival at the memory device 10 due to differences in propagation times, such as may be produced by routing differences between the command clock bus and the data clock bus.

[0005] Control data CD1-CDN arrive at respective input terminals 12 substantially simultaneously with pulses of the reference control clock signal CCLKREF and are latched in respective control data latches 16. However, if the device attempts to latch the control data CD1-CDN immediately upon the edge of the reference clock signal CCLKREF, the control data may not have sufficient time to develop at the input terminal 12. For example, a voltage corresponding to a first logic state (*e.g.,* a "0") at the input terminal 12 may not change to voltage corresponding to an opposite logic state (*e.g.,* a "1") by the time the data are latched. To allow time for the control data CD1-CDN to develop fully at the input terminal 12, the control data are latched at a delayed time relative to the reference control clock signal CCLKREF. To provide a clock edge to trigger latching of the commands CD1-CDN at the delayed time t_1, a delay circuit 18 delays the reference clock signal CCLKREF by a delay time T_{D1} to produce a first delayed clock signal CCLKD. Edges of the first delayed clock signal CCLKD activate the control data latches to latch the control data CD1-CDN at time t_1.

[0006] Data DA1-DAM arrive at the data terminals 14 substantially simultaneously with the reference data clock signal DCLKREF, as shown in the fourth and fifth graphs of Figure 2. Respective data latches 20 latch the data DA1-DAM. As with the control data CD1-CDN, it is desirable that the data DA1-DAM be latched with a slight delay relative to transitions of the reference data clock DCLKREF to allow time for signal development at the data terminals 14. To provide a delayed clock edge, a delay block 22 delays the reference data clock signal DCLKREF to produce a phase-delayed data clock DCLK1 that is delayed relative to the reference data clock signal DCLKREF by the delay time T_{D1}.

[0007] For latching both control data CD1-CDN and data DA1-DAM, it is often desirable to allow some adjustment of the phase delay. For example, if the clock frequencies change, the duration of the subperiods will change correspondingly. Consequently, the delayed clocks CCLKD, DCLKD may not allow sufficient signal development time before latching the control data or data. Also, variations in transmission times of control data, data, or clock signals may cause shifts in arrival times of control data CD1-CDN or data DA1-DAM relative to the clock signals CCLKREF, DCLKREF of the memory device.

[0008] One possible approach to producing a variable delay control clock CCLKD employs a delay-locked loop 38 driven by the reference command clock CCLKREF, as shown in Figure 3. The reference control clock signal CCLKREF is input to a conventional multiple output variable delay circuit 40 such as that described in Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE Journal of Solid-State Circuits 31*(11):1723-1732, November 1996. The delay circuit 40 is a known circuit that outputs multiple delayed signals CCLK1-CCLKN with increasing lags relative to the reference signal CCLKREF. The delays of the signals CCLK1-CCLKN are variable responsive to a control signal V_{CON} received at a control port 42.

[0009] A feedback circuit 44 formed from a comparator 46 and an integrator 48 produces the control signal V_{CON}. The feedback circuit 44 receives the reference

control clock signal CCLKREF at one input of the comparator 46 and receives one of the output signals CCLKN from the delay circuit 40 as a feedback signal at the other input of the comparator 46. The comparator 46 then outputs a compare signal V_{COMP} that is integrated by the integrator 48 to produce the control signal V_{CON}.

[0010] As is known, the control signal V_{CON} will depend upon the relative phases of the reference control clock signal CCLKREF and the feedback signal CCLKN. If the feedback signal CCLKN leads the reference control clock signal CCLKREF, the control signal V_{CON} increases the delay of the delay circuit 40, thereby reducing the magnitude of the control signal V_{CON} until the feedback signal CCLKN is in phase with the reference signal CCLKREF. Similarly, if the feedback signal CCLK lags the reference signal CCLKREF, the control signal V_{CON} causes the delay circuit 40 to decrease the delay until the feedback voltage CCLKN is in phase with the reference voltage CCLKREF.

[0011] A similar delay-locked loop 50 produces the delayed data clock signals DCLK1-DCLKN in response to the reference data clock signal DCLKREF. However, unlike the reference control clock signal CCLKREF, the reference data clock signal DCLKREF is discontinuous. Typically, the reference data clock signal DCLKREF arrives in bursts of clock pulses as a block: of data is accessed. Between bursts, the reference data clock signal DCLKREF is relatively inactive such that the delay-locked loop 50 may lose its lock. Consequently, when bursts arrive, the delays of the delayed data clocks DCLK1-DCLKN may not be properly adjusted by the delay-locked loop 50 and the data DA1-DAM may have insufficient or excessive development time at the data bus before latching.

[0012] From EP-A2-0 476 585 a reference delay generator has come to be known, comprising a delay-locked loop consisting of a primary variable delay block formed by a voltage controlled delay line and of a comparator formed by a phase difference detection circuit, a charge pump circuit, and a capacitor. EP '585 also discloses a secondary variable delay block formed by another voltage controlled delay line, which is also controlled by the output voltage of the comparator formed by said phase difference detection circuit, said charge pump circuit, and said capacitor.

[0013] The present invention provides for a memory device having the features of claim 1.

[0014] The invention also provided for a method of controlling the latching of commands and data defined by claim 3.

[0015] A first set of the clock signals is produced by a delay-locked loop in response to the reference clock signal. A delay block in the delay-locked loop receives the reference clock signal and produces a plurality of phase delayed signals at the clock frequency. One of the phase delayed signals is fed back to a comparator where the feedback signal is compared to the reference clock signal. The output of the comparator is then filtered and applied to a control input of the delay block to adjust the delay of the delay block. The delay-locked loop thus produces a plurality of output signals having fixed phases relative to the reference clock signal.

[0016] In addition to the delay-locked loop, the clock generator also includes a secondary delay block having a clock input fed by the secondary clock signal. The control input of the secondary delay block receives the control signal from the comparator, such that the comparator output controls both of the delay blocks. The secondary delay block outputs a plurality of secondary delayed signals each having a respective delay relative to the secondary clock signal. By controlling the variable delays of the secondary delayed signals with the output of the delay-locked loop driven by the reference clock signal, the secondary delay signals can remain delay-locked even though the secondary clock signal is a discontinuous data clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017]

Figure 1 is a block diagram of a prior art memory system including a memory device and memory controller linked by control data and data bases.

Figure 2 is a signal timing diagram showing timing of commands, data, and clock signals in the memory system of Figure 1.

Figure 3 is a block diagram of a pair of delay-locked loops separately driven by control and data reference clock signals according to prior art.

Figure 4 is a block diagram of a memory system according to the invention, including a memory device having a clock generator circuit where a delay-locked loop generates command clock signals in response to a reference clock signal and a variable delay block coupled to the delay-locked loop generates data clock signals in response to a reference data clock signal

Figure 5 is a block diagram of a computer system including the memory system of Figure 4.

DETAILED DESCRIPTION OF THE INVENTION

[0018] As shown in Figure 4, a memory system 52 includes a memory device 58 that operates under control of a memory controller 53. The memory controller 53 controls the memory device 58 through control data CD1-CDN and a reference clock signal CCLKREF, carried by a control data bus 54 and a clock bus 55, respectively. The memory controller 53 provides data DA1-DAM to the memory device 58, synchronously with a data clock signal DCLKREF over a data bus 56 and a data clock bus 57, respectively.

[0019] The memory device 58 includes a latching circuit 60 that operates under control of a logic control cir-

cuit 61. The latching circuit 60 is formed from a delay-locked loop 62, a variable slave delay circuit 64, control data latches 66, and data latches 68. The control data latches 66 receive control data CD1-CDN from the control data bus 54 and the data latches 68 receive data DA1-DAM on the data bus 56. Additionally, the latching circuit 60 receives the reference control clock signal CCLKREF and the reference data clock signal DCLKREF from the respective clock buses 55, 57.

[0020] As discussed above, the reference control clock signal CCLKREF is a continuous clock signal that drives the delay-locked loop 62 at a frequency f_{CCLK}. Like the delay locked loop 38 described above with reference to Figure 3, the delay-locked loop 62 is formed from the variable delay circuit 40, comparator 46, and integrator 48. The variable delay circuit 40 is formed from a multitap variable delay line 70 of conventional construction and a selector switch 71. The delay circuit 40 provides several delayed clock signals CCLK1-CCLKN, each at the frequency f_{CCLK} and each delayed by a respective time delay relative to the reference control clock signal CCLKREF. The selector switch 71, under control of the logic control circuit 61, couples one of the outputs of the variable delay line 70 to the control data latches form the delayed reference clock signal CCLKD. The logic controller 61 selects the switch position to select a delayed clock signal CCLK1-CCLKN that has a pulse delayed by approximately half of the data clock period relative to the control clock CCLKREF as the delayed clock signal CCLKD. The logic controller 61 is able to vary the switch position to accommodate changes in clock period that may occur as a result of operating frequency changes. As discussed above, the delayed reference clock signal CCLKD activates the control data latches 66, thereby latching control data CD1-CDN. The latched control data CD1-CDN is then made available to the logic control circuit 61.

[0021] Unlike the circuit of Figure 3, the latching circuit 60 of Figure 4 does not employ a second delay-locked loop to produce the delayed data clock signal DCLKD. Instead, the reference data clock signal DCLKREF drives a slave delay circuit 64 formed from a second variable delay line 82 and a second selector switch 83. The delay of the second delay line 82 is controlled by applying the control signal V_{CON} from the integrator 48 to the control input 84 of the second delay line 82. The overall delay of the second delay line 82 is substantially equal to that of the variable delay line 70 of the delay-locked loop 62. However, the number of subperiods may differ between the delay lines 70, 82. The second selection switch 83 couples one of the delayed data clock signals DCLK1-DCLKN to the data latches 68 to produce the delayed data clock DCLKD, which is delayed relative to the data clock DCLKREF by the delay time T_{D1}. The delayed data clock DCLKD activates the latches 68, thereby latching data DA1-DAM arriving at the input data bus 72. The latched data DA1-DAM is then made available by the latches 68 to a memory array 82 through read/write circuitry 84.

[0022] One skilled in the art will recognize that the latching circuit 60 takes advantage of the matching clock periods T of the reference clock CCLKREF and the reference data clock DCLKREF to eliminate the delay-locked loop 50 of Figure 3. Because the delay time T_{D1} of the delayed data clock DCLKD is controlled by the delay-locked loop 62 driven at the same frequency as the reference data clock DCLKREF, the delayed data clock DCLKD has a fixed phase relationship relative to the discontinuous reference data clock signal DCLKREF without requiring locking to the discontinuous reference data clock DCLKREF.

[0023] By eliminating the delay-locked loop 50 of Figure 3 and establishing the delay time T_{D1} with reference to the reference clock signal CCLKREF, the memory system 52 establishes the delay time T_{D1} with reference to a continuous signal (CCLKREF) rather than a discontinuous signal (DCLKREF). Consequently, the memory system 52 provides a continuously controlled time delay T_{D1} while eliminating the difficulties in attempting to lock the delay-locked loop 50 to the discontinuous data clock signal DCLKREF.

[0024] As noted above, the selector switches 71, 83 selectively couple the outputs of the variable delay circuits 40, 64 to the respective latches 66, 68. The positions of the selector switches 71, 83 are selected by the logic control circuit 61. Preferably, the selector switch position is programmed into the logic controller 61 when the memory device 58 is produced. However, where the memory device 58 may be used at more than one frequency or where the arrival times of data or commands may vary relative to their respective reference clocks CCLKREF, DCLKREF, the memory controller 53 may command the logic control circuit 61 to define a revised selection switch position. Thus, the use of a multi-tap variable delay line 70 in combination with the selector switches 71, 83 allows the memory device 58 to be "tuned" for varying operating conditions or frequencies.

[0025] Figure 5 is a block diagram of a computer system 200 that contains the memory controller 53 and three of the memory devices 58 of Figure 4. The computer system 200 includes a processor 202 for performing computer functions such as executing software to perform desired calculations and tasks. The processor 202 also includes command, address and data buses 210 to activate the memory controller 53, thereby controlling reading from and writing to memory devices 58. One or more input devices 204, such as a keypad or a mouse, are coupled to the processor 202 and allow an operator to manually input data thereto. One or more output devices 206 are coupled to the processor 202 to display or otherwise output data generated by the processor 202. Examples of output devices include a printer and a video display unit. One or more data storage devices 208 are coupled to the processor to store data on or retrieve data from external storage media (not shown). Examples of storage devices 208 and storage

media include drives that accept hard and floppy disks, tape cassettes and compact-disk read-only memories.

[0026] While the invention has been described herein by way of exemplary embodiments, various modifications may be made without departing from the spirit and scope of the invention. For example, although the computer system 200 of Figure 5 contains only three memory devices 58, a larger or smaller number of memory devices 58 may be included within the computer system 200. Similarly, although the feedback portion of the delay-locked loop 62 is presented as containing only a comparator 46 and integrator 48, other circuitry may be used to control the variable delay lines 70, 82. Also, one skilled in the art will understand that other feedback elements may replace the comparator 46 and integrator 48. For example, the comparator 46 can be replaced by any know phase comparing or detecting circuit and the integrator 48 may be replaced by a conventional loop filter. Additionally, where the memory device 58 is operated such that control data and data are latched at a constant phase relative to the reference clocks CCLKREF, DCLKREF, the variable delay lines 70, 82 may have only one output. Also, although the combination of the delay-locked loop 62 and the additional variable delay block 82 are described herein as part of a latching circuit 60, a variety of other circuits may be developed incorporating this combination. Moreover, although the outputs of the variable delay lines 70, 82 are shown herein as driving the latches 66, 68, the outputs may also drive other circuitry in the memory device 58 to control timing of operations in addition to, or other than, latching. Further, although the exemplary embodiment described herein uses a delay locked loop 62 to lock to the reference clock signal CCLKREF, one skilled in the art could easily adapt the circuits described herein to employ a phase-locked loop for locking. Accordingly, the invention is not limited except as by the appended claims.

Claims

1. A memory device adapted to receive data and commands at a reference frequency, the memory device comprising:

   a) a data input terminal (DA1-DAM);
   b) a command input terminal (CD1-CDN);
   c) a primary delay-locked loop including

      ca) a reference clock terminal adapted to receive a reference clock signal (CCLKREF) at the reference frequency;
      cb) a comparator (46, 48) having

      - a first input terminal coupled to the reference clock terminal and adapted to receive the reference clock signal (CCLKREF),
      - a second input terminal receiving a delayed clock signal (CCLKN), and
      - the comparator (46, 48) being responsive to, output a compare signal (V_{CON}) indicative of a relationship between the reference clock signal (CCLKREF) received at the first input and the delayed clock signal (CCLKN) received at the second input terminal; and

      cc) a primary variable delay block (70) having

      - a primary control input coupled to the comparator (46, 48) output,
      - a primary clock input terminal coupled to the reference clock terminal and
      - a first delay output coupled to the second input terminal of the comparator (46, 48),
      - a second delay output;
      - the primary variable delay block (70) producing the delayed clock signal (CCLKN) responsive to the reference clock signal (CCLKREF) with a primary delay that varies responsive to the compare signal (V_{CON}) at the primary control input;

   d) a command latch (66) having a clocking input coupled to a secondary delay output and a command input coupled to the command input terminal (CD1-CDN);
   e) a secondary clock terminal adapted to receive a secondary clock signal (DCLKREF) at a secondary clock frequency;
   f) a secondary delay block (82) having

      fa) a secondary control input terminal coupled to the comparator (46, 48) output,
      fb) a secondary clock input coupled to the secondary clock terminal, and a secondary delay output,
      fc) the secondary delay block producing a first secondary delayed signal (DCLKD) at the secondary delay output at the secondary frequency with a secondary delay that varies responsive to the compare signal (V_{CON}) at the secondary control input; and

   g) a data latch (68) having a data clocking input coupled to the secondary delay output and a data input coupled to the data input terminal (DA1-DAM).

2. The memory device of claim 1 wherein

a) the primary variable delay block (70) further includes a second delay output that provides a second secondary delayed signal with a second primary delay between the primary clock input and the second delay output that varies responsive to the compare signal (V_{CON}) at the primary control input,
b) the second primary delay being different than the first primary delay.

3. A method of controlling the latching of commands and data in a memory device responsive to respective command clock signals and data clock signals having respective clock frequencies and clock phases, the method comprising the steps of:

a) producing a delayed command clock signal in response to the command clock signal, the delayed command clock signal being delayed from the command clock signal by a command delay time;
b) producing a delayed data clock signal in response to the data clock signal, the delayed data clock signal being delayed from the data clock signal by a data delay time;
c) comparing a phase of the delayed command clock signal to the phase of the command clock signal;
d) in response to the step of comparing the phases, adjusting the command delay time to produce an adjusted delayed command clock signal;
e) in response to the step of comparing the phases, adjusting the data delay time to produce an adjusted delayed data clock signal;
f) latching the data in response to the adjusted delayed data clock signal; and
g) latching the commands in response to the adjusted delayed command clock signal.

4. The method of claim 3 wherein the step of producing a delayed data clock signal includes the step of providing the data clock signal to a delay line and the step of adjusting the data delay time includes adjusting delay of the delay line.

Patentansprüche

1. Speichervorrichtung zum Empfangen von Daten und Befehlen bei einer Referenzfrequenz, umfassend:

a) einen Dateneingangsanschluß (DA1-DAM);
b) einen Befehlseingangsanschluß (CD1-CDN);
c) eine primäre Verzögerungsregelschleife, umfassend:

ca) eine Referenztakt-Anschluß zum Empfangen eines Referenztaktsignals (CCLKREF) mit der Referenzfrequenz;
cb) einen Vergleicher (46, 48) mit

- einen ersten Eingangsanschluß, angeschlossen an den Referenztaktanschluß und ausgebildet für den Empfang des Referenztaktsignals (CCLKREF),
- einen zweiten Eingangsanschluß zum Empfangen eines verzögerten Taktsignals (CCLKN), und
- wobei der Vergleicher (46, 48) anspricht auf die Ausgabe eines Vergleichssignals (V_{CON}), welches kennzeichnend ist für eine Beziehung zwischen dem Referenztaktsignal (CCLKREF), das an dem ersten Eingang empfangen wird, und dem verzögerten Taktsignal (CCLKN), das an dem zweiten Eingangsanschluß empfangen wird; und

cc) einen primären variablen Verzögerungsblock (70), umfassend:

- einen primären Steuereingang, angeschlossen an den Ausgang des Vergleichers (46, 48),
- einen Primär-Takteingangsanschluß, gekoppelt mit dem Referenztaktanschluß, und
- einen ersten Verzögerungsausgang, der an den zweiten Eingangsanschluß des Vergleichers (46, 48) gekoppelt ist,
- einen zweiten Verzögerungsausgang,
- wobei der primäre variable Verzögerungsblock (70) das verzögerte Taktsignal (CCLKN) ansprechend auf das Referenztaktsignal (CCLKREF) mit einer Primärverzögerung erzeugt, die abhängig von dem Vergleichssignal (V_{CON}) an dem Primärsteuereingang variiert;

d) einen Befehlszwischenspeicher (66), der mit einem Takteingang an einen Sekundär-Verzögerungsausgang und mit einem Befehlseingang an den Befehlseingangsanschluß (CD1-CDN) gekoppelt ist;
e) einen Sekundärtaktanschluß zum Empfangen eines Sekundärtaktsignals (DCLKREF) mit einer zweiten Taktfrequenz;
f) einen sekundären Verzögerungsblock (82), umfassend:

fa) einen sekundären Steuereingangsanschluß, der an den Ausgang des Vergleichers (46, 48) gekoppelt ist,
fb) einen Sekundärtakteingang, der an den Sekundärtaktanschluß gekoppelt ist, und einen Sekundär-Verzögerungsausgang,
fc) wobei der Sekundärverzögerungsblock ein erstes sekundäres verzögertes Signal (DCLKD) an dem Sekundärverzögerungsausgang mit der Sekundärfrequenz erzeugt, wobei eine Sekundärverzögerung ansprechend auf das Vergleichssignal (V_{CON}) an dem Sekundärsteuereingang schwankt; und

g) einen Datenzwischenspeicher (68) mit einem Datentakteingang, gekoppelt an den Sekundärverzögerungsausgang, und mit einem Dateneingang, der mit dem Dateneingangsanschluß (DA1-DAM) gekoppelt ist.

2. Speichervorrichtung nach Anspruch 1, bei dem

a) der primäre variable Verzögerungsblock (70) außerdem einen Sekundärverzögerungsausgang aufweist, der ein zweites sekundäres verzögertes Signal mit einer zweiten Primärverzögerung zwischen dem Primärtakteingang und dem Sekundärverzögerungsausgang liefert, die ansprechend auf das Vergleichssignal (V_{CON}) an dem Primärsteuereingang schwankt,
b) die zweite Primärverzögerung sich von der ersten Primärverzögerung unterscheidet.

3. Verfahren zum Steuern des Zwischenspeichers von Befehlen und Daten in einer Speichervorrichtung in Abhängigkeit von jeweiligen Befehlstaktsignalen bzw. Datentaktsignalen, die jeweilige Taktfrequenzen und Taktphasen besitzen, umfassend folgende Schritte:

a) Erzeugen eines verzögerten Befehlstaktsignals ansprechend auf das Befehlstaktsignal, wobei das verzögerte Befehlstaktsignal gegenüber dem Befehlstaktsignal um eine Befehlsverzögerungszeit verzögert ist;
b) Erzeugen eines verzögerten Datentaktsignals in Abhängigkeit des Datentaktsignals, wobei das verzögerte Datentaktsignal gegenüber dem Datentaktsignal um eine Datenverzögerungszeit verzögert ist;
c) Vergleichen einer Phase des verzögerten Befehlstaktsignals mit der Phase des Befehlstaktsignals;
d) abhängig vom Schritt des Vergleichens der Phasen, Einstellen der Befehlsverzögerungszeit, um ein eingestelltes verzögertes Befehlstaktsignal zu erzeugen;
e) ansprechend auf den Schritt des Vergleichs der Phasen, Einstellen der Datenverzögerungszeit, um ein eingestelltes verzögertes Datentaktsignal zu erzeugen;
f) Zwischenspeichern der Daten in Abhängigkeit des eingestellten verzögerten Datentaktsignals; und
g) Zwischenspeichern der Befehle in Abhängigkeit des eingestellten verzögerten Befehlstaktsignals.

4. Verfahren nach Anspruch 3, bei dem der Schritt des Erzeugens eines verzögerten Datentaktsignals den Schritt beinhaltet, daß das Datentaktsignal auf eine Verzögerungsleitung gegeben wird, und den Schritt beinhaltet, daß das Einstellen der Datenverzögerungszeit das Einstellen der Verzögerung der Verzögerungsleitung beinhaltet.

Revendications

1. Dispositif de mémoire adapté pour recevoir des données et des commandes à une fréquence de référence, le dispositif de mémoire comprenant :

a) une borne d'entrée de données (DA1-DAM);
b) une borne d'entrée de commandes (CD1-CDN);
c) une boucle à retard verrouillé primaire comprenant

ca) une borne d'horloge de référence adaptée pour recevoir un signal d'horloge de référence (CCLKREF) à la fréquence de référence ;

cb) un comparateur (46, 48) comprenant

- une première borne d'entrée couplée à la borne de l'horloge de référence et adaptée pour recevoir le signal d'horloge de référence (CCLKREF),
- une seconde borne d'entrée recevant un signal d'horloge retardé (CCLKN), et
- le comparateur (46, 48) réagissant pour transmettre un signal de comparaison (V_{CON}) indicatif d'une relation entre le signal d'horloge de référence (CCLKREF) reçu au niveau de la première entrée et le signal d'horloge retardé (CCLKN) reçu au niveau de la seconde borne d'entrée ; et

cc) un bloc à retard variable primaire (70) comprenant

- une entrée de contrôle primaire couplée à la sortie du comparateur (46, 48),
- une borne d'entrée d'horloge primaire couplée à la borne d'horloge de référence, et
- une première sortie retardée couplée à la seconde borne d'entrée du comparateur (46, 48),
  une seconde sortie à retard,
- le bloc à retard variable primaire (70) produisant le signal d'horloge retardé (CCLKN) en réaction au signal d'horloge de référence (CCLKREF) avec un retard primaire qui varie suivant le signal de comparaison (V_{CON}) au niveau de l'entrée de contrôle primaire ;

d) une bascule de commande (66) disposant d'une entrée de synchronisation couplée à une sortie à retard secondaire et d'une entrée de commande couplée à la borne d'entrée de commande (CD1-CDN) ;
e) une borne d'horloge secondaire adaptée pour recevoir un signal d'horloge secondaire (DCLKREF) à une fréquence d'horloge secondaire ;
f) un bloc à retard secondaire (82) possédant

fa) une borne d'entrée de contrôle secondaire couplée à la sortie du comparateur (46, 48);
fb) une entrée d'horloge secondaire couplée à la borne d'horloge secondaire, et une sortie à retard secondaire ;
fc) le bloc à retard secondaire produisant un premier signal retardé secondaire (DCLKD) au niveau de la sortie à retard secondaire à la fréquence secondaire avec un retard secondaire qui varie en réponse au signal de comparaison (V_{CON}) au niveau de l'entrée de contrôle secondaire ; et

g) une bascule de données (68) disposant d'une entrée de synchronisation de données couplée à la sortie à retard secondaire et d'une entrée de données couplée à la borne d'entrée de données (DA1-DAM).

2. Dispositif de mémoire de la revendication 1 dans lequel :

a) le bloc à retard variable primaire (70) comprend en outre une seconde sortie à retard qui fournit un second signal retardé secondaire avec un second retard primaire entre l'entrée d'horloge primaire et la seconde sortie à retard qui varie en réponse au signal de comparaison (V_{CON}) au niveau de l'entrée de contrôle primaire,

b) le second retard primaire étant différent du premier retard primaire.

3. Méthode de contrôle du déclenchement de commandes et de données dans un dispositif de mémoire en réponse à des signaux d'horloge de commande et des signaux d'horloge de données respectifs ayant des fréquences d'horloge et des phases d'horloge respectives, la méthode comprenant les étapes consistant à :

a) produire un signal d'horloge de commande retardé en réponse au signal d'horloge de commande, le signal d'horloge de commande retardé étant en retard d'un temps de retard de commande par rapport au signal d'horloge de commande ;

b) produire un signal d'horloge de données retardé en réponse au signal d'horloge de données, le signal d'horloge de données retardé étant en retard d'un temps de retard de données par rapport au signal d'horloge de données ;

c) comparer une phase du signal d'horloge de commande retardé à la phase du signal d'horloge de commande ;

d) en réponse à l'étape de comparaison des phases, ajuster le temps de retard de commande pour produire un signal d'horloge de commande retardé ajusté ;

e) en réponse à l'étape de comparaison des phases, ajuster le temps de retard de données pour produire un signal d'horloge de données retardé ajusté ;

f) déclencher les données en réponse au signal d'horloge de données retardé ajusté ; et

g) déclencher les commandes en réponse au signal d'horloge de commande retardé ajusté.

4. Méthode de la revendication 3 dans laquelle l'étape consistant à produire un signal d'horloge de données retardé comprend l'étape consistant à transmettre le signal d'horloge de données à une ligne à retard et dans laquelle l'étape consistant à ajuster le temps de retard de données comprend l'ajustement du retard de la ligne à retard.

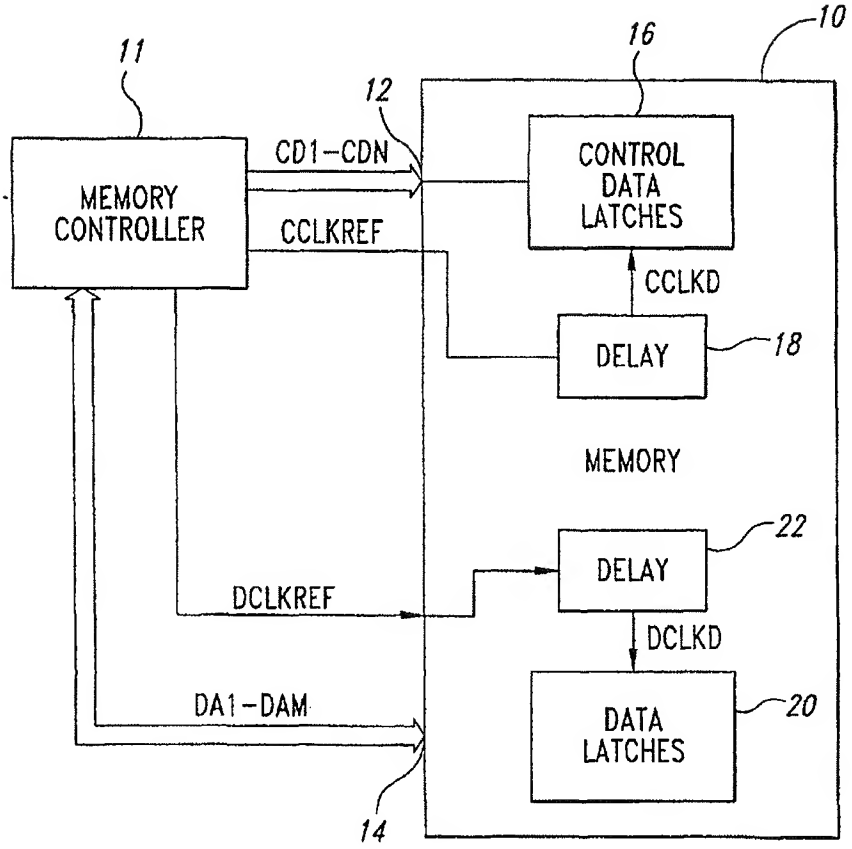

Fig. 1
(Prior Art)

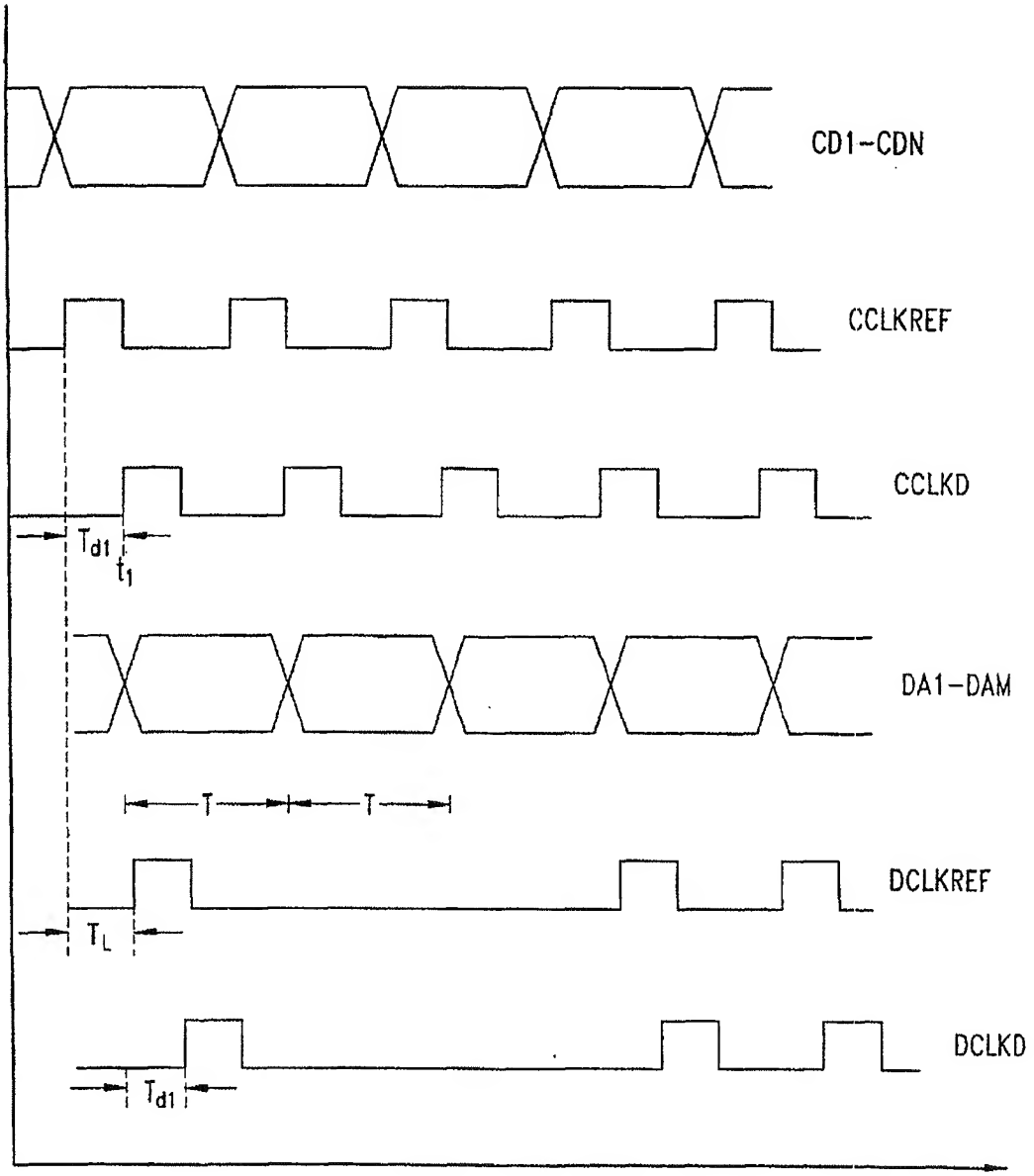

Fig. 2

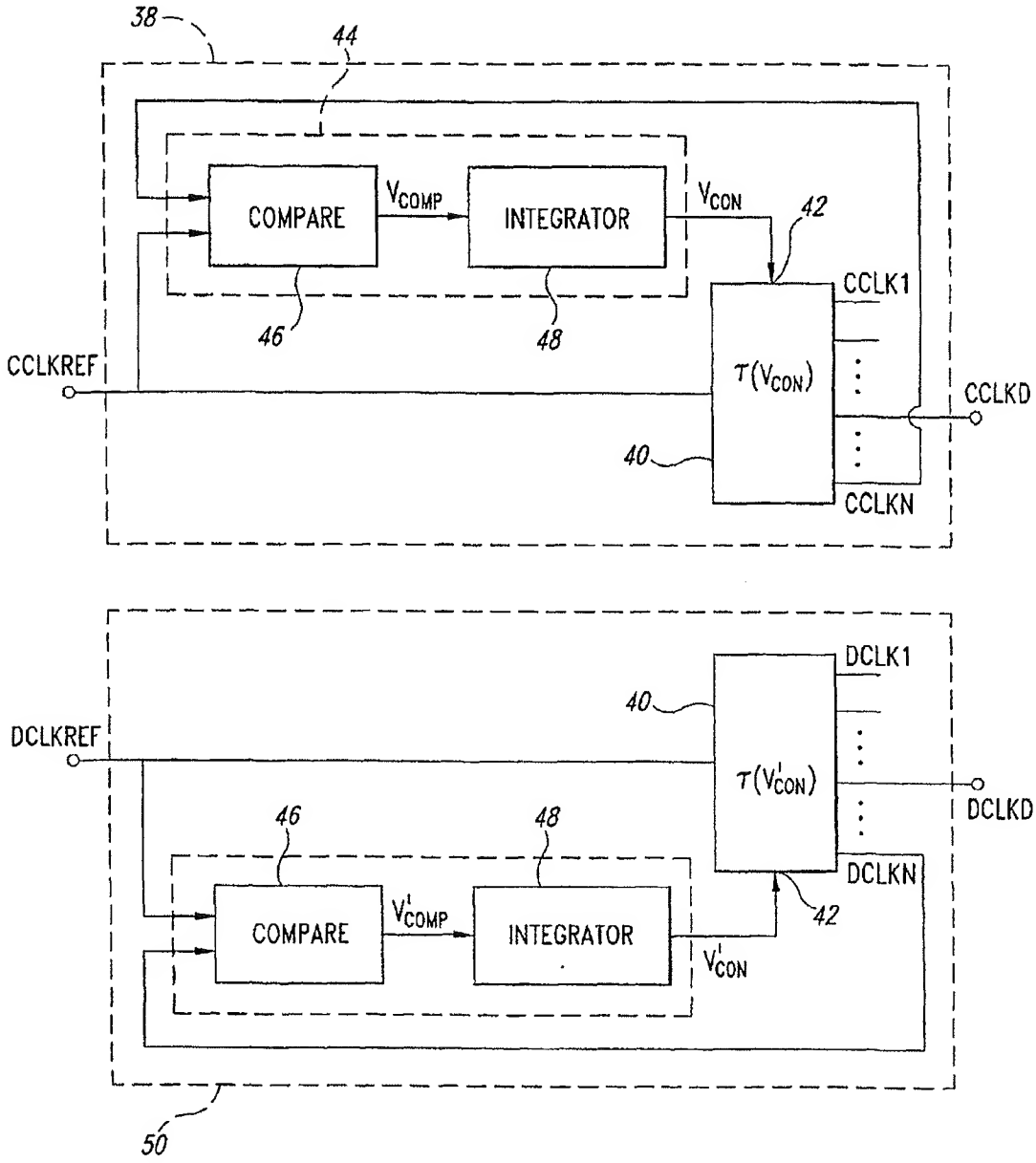

Fig. 3
(Prior Art)

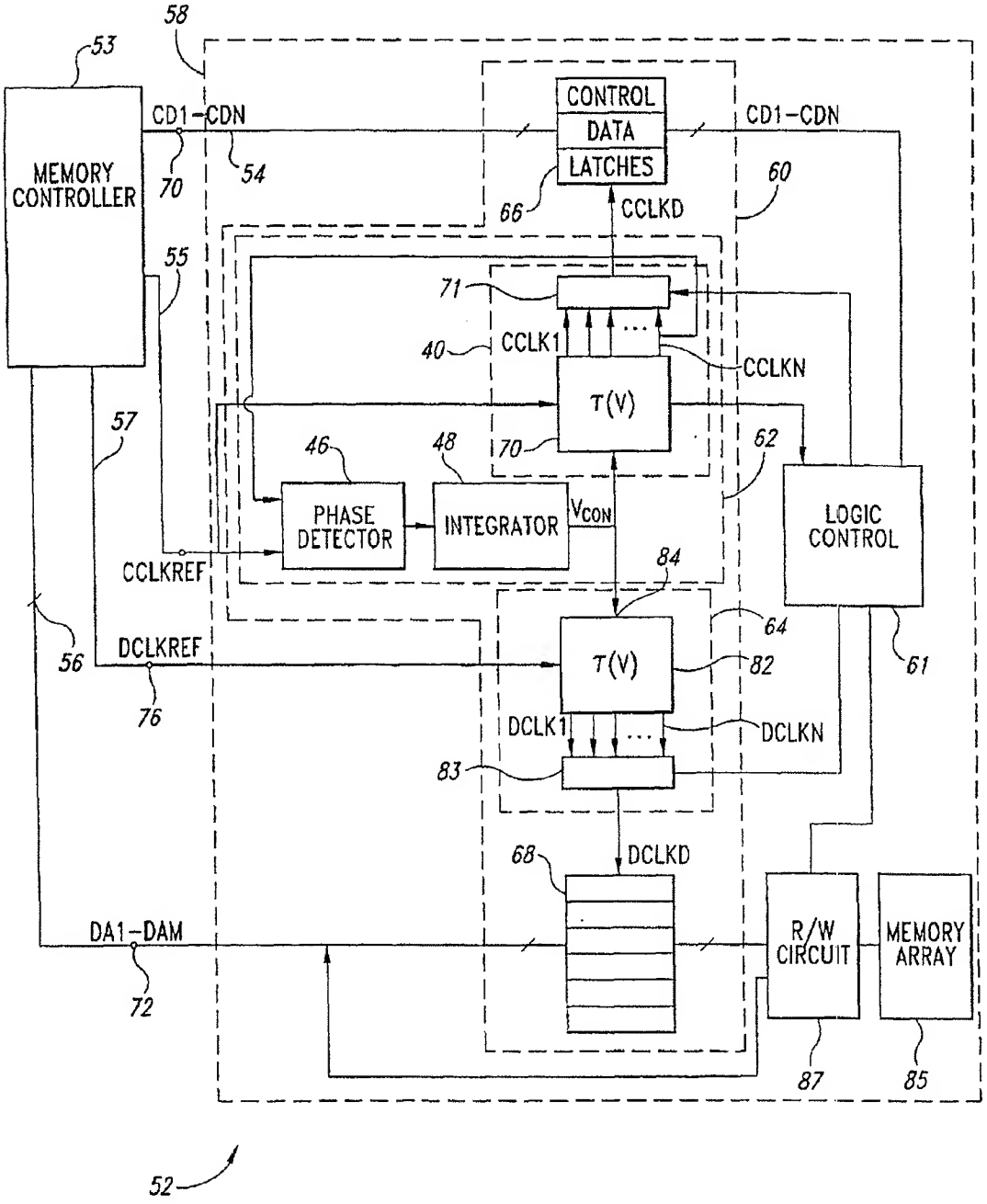
58
53
MEMORY CONTROLLER
CD1-CDN
70
54
CONTROL
DATA
LATCHES
66
CCLKD
CD1-CDN
60
55
71
40
CCLK1
CCLKN
T(V)
57
46
48
70
62
PHASE DETECTOR
INTEGRATOR
VCON
LOGIC CONTROL
CCLKREF
84
64
56
DCLKREF
T(V)
82
61
76
DCLK1
DCLKN
83
68
DCLKD
DA1-DAM
R/W CIRCUIT
MEMORY ARRAY
72
87
85
52

Fig. 4

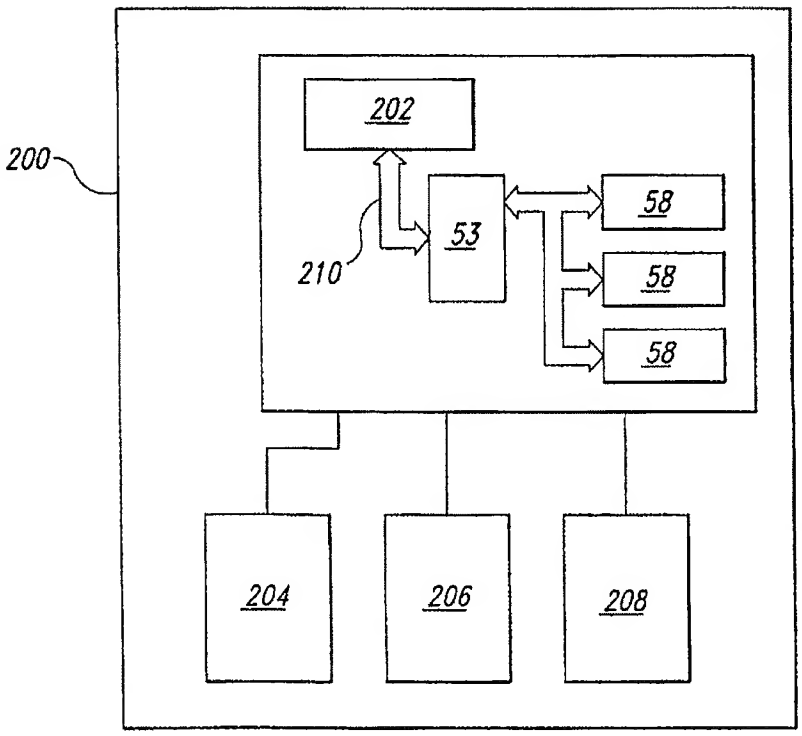

Fig. 5